BEng Project Mission Statement

Acceleration of LU Decomposition on FPGAs

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# Background

Simulation Program with Integrated Circuit Emphasis or SPICE has now been widely used in the IC design and verification. Solving of sparse matrices often takes up most of the SPICE simulation time. Lower–upper (LU) decomposition is the most commonly used method to solve matrices. It factorizes a matrix into two factors – a lower triangular matrix *L* and an upper triangular matrix *U*. In this way, we only need to solve triangular systems to get results. However, the sparse-matrix computation is hard to parallelize on regular processors due to the irregular structure of the matrices. Modern FPGAs, however, have the potential to compute these hard-to-parallelise problems more efficiently due to its flexible reconfigurability.

# Aim & Tasks

Implement LU Decomposition on FPGAs and accelerate it.

* To implement LU decomposition with C++.
* To implement LU decomposition on FPGA.
* Test the power consumption and efficiency of the algorithm on FPGA.
* Accelerate the LU decomposition by parallelization and make it robust enough for circuit simulation application.
* Produce a parallel FPGA-based Matrix Solver.

# Background Knowledge

* C++ is designed with an orientation towards system programming and embedded. It offers a direct hardware mapping and can be synthesized into FPGA. Modern C++ has also provided parallel version of many algorithms.
* Verilog is a hardware description language. It is commonly used in design and verification of digital circuit in register-transfer level and can be physically realized by synthesis software.

# Resources

* Xilinx Vitis

The Vitis unified software platform is a free new tool that combines all aspects of Xilinx software development into one unified environment. It enables accelerated applications on various Xilinx platforms including FPGAs. It is easy to get from Xilinx official website.

* Intel oneAPI

oneAPI is a cross-industry, open, standards-based unified programming model that delivers a common developer experience across accelerator architectures. It provides optimized compilers, libraries, frameworks and analysis tools for development on CPUs, GPUs and FPGAs. It provides free access through Intel official website.

The supervisor and student are satisfied that this project is suitable for performance and assessment in accordance with the guidelines of the course documentation.

Signed

Yichen Zhang: ..................................

Dr Danial Chitnis: .............................

Date: ................